REMARKS/ARGUMENTS

In the Final Office Action dated September 25, 2003, Claims 1-30 are pending. Claims 1-30 stand rejected. A response to the Office Action was filed and an advisory action was issued. In the Advisory Action, the amendment to claim 7 was accepted. However, the arguments in response the Office Action were deemed to be non-persuasive.

In this response, no claim has been canceled. Claims 1, 6, 12, 18, and 24 have been amended. No new matter has been added. Reconsideration of the present application as amended is respectfully requested.

Claims 1-3, 5-6, 9-12, 14-16, 17-19, and 21-30 are rejected under 35 U.S.C. 102(b) as being anticipated by the Intel 440BX AGPset: 82443BX Host Bridge/Controller ("the Intel 82443BX"). In view of the foregoing amendments, Applicant respectfully submits that claims 1-30 are not anticipated by the Intel 82443BX. Specifically, independent claim 1 recites as follows:

> 1. An apparatus, comprising:
> an interface for directly coupling to a host bus having one or more processors;
> a device coupled to the interface to perform one or more functions, said device appearing as a virtual PCI device, other than a virtual host-to-PCI bridge, logically residing on a PCI bus that is coupled to the host bus through a host-to-PCI bridge; and
> a monitor circuit coupled to said interface and said device to track host bus cycles initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device, and to generate one or more control signals to enable the device to respond, as the virtual PCI device, to said one or more of said identified host bus cycles targeted to said virtual PCI device.
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> (Emphasis added)

It is respectfully submitted that independent claim 1 includes a device (e.g., a host bus device) directly coupled to a host bus having one or more processors (e.g., a processor bus) and the device appears as a virtual PCI device other than a virtual host-to-PCI bridge logically residing on a PCI bus that is coupled to the host bus through a host-to-PCI bridge.

Independent claim 1 further includes a monitor circuit coupled to the device to monitor the host bus cycles targeted to the logical virtual PCI device and to generate a control signal to enable the virtual PCI device to respond to the host bus cycles. That is, the device is physically located on a processor bus along with one or more processors. However, the device appears as a PCI device (other than a host-to-PCI bridge) on a PCI bus behind the host-to-PCI bridge (which is similar to the host-to-PCI bridge of the Intel 82443BX). The monitor circuit enables the device to respond as if the device is a PCI device on a PCI bus behind the host-to-PCI bridge. Applicant respectfully submits that the Intel 82443BX fails to disclose the above limitations.

Rather, the Intel 82443BX discloses a host bridge having a host-to-PCI interface and a host-to-AGP interface (see, page iv of the Intel 82443BX), where the host-to-AGP interface is still considered as a host-to-PCI bridge (see, page 3-4 of the Intel 82443BX). It appears that the Examiner interprets the host-to-PCI interface or the host-to-AGP interface of the Intel 82443BX as the host bus device as claimed in the present application. Specifically, the Examiner stated:

> "In regards to claim 1, 12, 18, 21, and 24-25: 82443BX teaches an apparatus comprising: an interface (Page iv Host Interface) for directly coupled to a host bus (Host bus) having one or more processors (Page iii multiprocessor support); a device (Page 3-5 "Virtual Host-to-PCI Bridge" identified as device 1 also the AGP interface note 82443BX also has a device 0) coupled to the interface to perform one or more functions (AGP interface functions page 3-1), said device appearing as a virtual PCI device (82443BX calls it virtual) logically residing on a PCI bus (PCI bus 0) that is coupled to the host bus through a host-to-PCI bridge (Host-to-PCI bridge); and a monitor circuit (Decoder Page 1-2) coupled to said interface and said device to track host bus cycles (Host cycles) initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device, to said one or more said control signals (DEVSEL#) to respond, as the virtual PCI device, to said one or more said identified host bus cycles targeted to said virtual PCI device."
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> (9/25/2003 Office Action, page 3, Emphasis added)

Applicant respectfully disagrees. Applicant respectfully submits that the present invention as claimed relates to a host bus device that physically sits on a host bus, but logically appears as a logical PCI device sitting on a PCI bus behind a host-to-PCI bridge (but not part of the bridge or a host-to-PCI bridge, such as, host-to-AGP bridge). In contrast, the Intel 82443BX is a bridge that provides interfaces to PCI buses and/or AGP devices, etc. The host-to-PCI and host-to-AGP interfaces are part of the host bridge coupling the host bus to other buses (e.g., a host-to-PCI bridge). Such interfaces are not the host bus devices as claimed in the present application that physically sit on the host bus and responds to the host bus cycles as a virtual PCI device. See, for example, Figure 1-1 on page 1-2 of the Intel 82443BX. Specifically, the Intel 82443BX states:

> "The 82443 BX supports two bus interfaces: PCI (referred as Primary PCI) and AGP (referenced as AGP). The AGP interface is treated as a second PCI bus from the configuration point of view."
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> (Page 3-5 of the Intel 82443BX).

Thus, none of the interfaces can be considered as host bus devices as claimed in the present application. Applicant respectfully submits that, at most, the Intel 82443BX bridge as a whole, which couples a host bus to other buses, may be considered as a host bus device directly coupled to the host bus or a host-to-PCI or a host-to-AGP bridge, where the host-to-AGP bridge is still considered as a host-to-PCI bridge (see, page 3-4 of the Intel 82443BX). However, the Intel 82443BX bridge cannot be considered as a virtual PCI device, other than a virtual host-to-PCI bridge, logically residing at a PCI bus behind a host-to-PCI bridge (within itself).

Even if, for the sake of the argument, that the host-to-PCI interface or the host-to-AGP interface may be considered as a host bus device directly coupled to a host bus, the Intel 82443BX still lacks a monitor circuit to track host bus cycles initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to

the virtual PCI device (e.g., the alleged host bus device, such as the host-to-PCI interface or the host-to-AGP interface), and to generate one or more control signals to enable the device (again, the alleged host bus device, such as the host-to-PCI interface or the host-to-AGP interface) to respond, as the virtual PCI device, to said one or more of said identified host bus cycles targeted to said virtual PCI device.

The Examiner contends that a decoder of page 1-2 of the Intel 82443BX is the monitor circuit as claimed in the present application and the DEVSEL# signal is the control signal to enable a virtual PCI device to respond to the targeted host bus cycles. Applicant respectfully disagrees. The decoder of the Intel 82443BX does not track the host bus cycles that are targeted to the alleged host bus device when the device is considered either the host-to-PCI interface or the host-to-AGP interface. Rather, the alleged decoder decodes memory and IO cycles targeted to the memory or IO device (including the AGP device). Specifically, the Intel 82443BX states:

> "Host-initiated I/O cycles are decoded to PCI, AGP or PCI configuration space. Host-initiated memory cycles are decoded to PCI, AGP (prefetchable or non-prefetchable space) or DRAM (including AGP aperture memory). For memory cycles (host, PCI or AGP initiated) that target the AGP aperture space in DRAM, the 82443BX translates the address using the AGP address translation table. Other host cycles forwarded to AGP are defined by the AGP address map.
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> (the Intel 82443BX, page 1-2, emphasis added).

Thus, importantly, Applicant respectfully submits that the host bus cycles are not targeted to the host-to-PCI interface or host-to-AGP interface. Rather, the host-to-PCI or host-to-AGP interface translates and forwards the host bus cycles from a host bus to PCI devices or AGP devices coupled to a PCI bus behind the host-to-PCI or the host-to-AGP bridge respectively, which is the target of the host bus cycles. However, the DEVSEL# signal is not a control signal that enables the host-to-PCI device or the host to AGP device to respond, as the virtual PCI device, to one or more of the identified host bus cycles targeted to

the virtual PCI device, because the host bus cycles are not targeted to the host-to-PCI or host-to-AGP bridge interface.

The AGP device asserts the DEVSEL# signal, not the host-to-PCI interface. Therefore, the monitor unit does not use the DEVSEL# signal to help the host-to-PCI interface to respond, but the other device coupled to the AGP interface. Therefore, for the reasons discussed above, independent claim 1 is not anticipated by the Intel 82443BX.

Independent claims 12, 18, and 24 include limitations similar to those referred by claim 1. Thus, for the reasons similar to those discussed above, claims 12, 18, and 24 are not anticipated by the Intel 82443BX.

Given that claims 2-11, 13-17, 19-23, and 25-30 depend from one of the above independent claims, it is respectfully submitted that 2-11, 13-17, 19-23, and 25-30 are also not anticipated by the Intel 82443BX. Withdrawal of the rejections is respectfully submitted.

Claims 4, 7, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel 82443BX. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,659,551 of Huott et al. ("Huott").

Applicant submits that Huott relates to a computer system element having a VLSI array with redundant areas and an ABIST system having mirror image fuse registers enabling scan of failed addresses to be used to replace hardware errors detected during the power-on tests at a customer location. It is respectfully submits that Huott also fails to disclose or suggest the limitations discussed above. Therefore, at least for the reasons similar to those discussed above, claims 4, 7-8, 13, and 20 are patentable over the Intel 82443BX in view of Huott. Withdrawal of the rejections is respectfully submitted.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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